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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,667	09/30/2004	Shu-Hua Kuo	13300-US-PA	,5666

31561 7590 04/25/2007
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

HE, AMY

ART UNIT	PAPER NUMBER
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2858

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

T.H

Office Action Summary

Application No.

10/711,667

Applicant(s)

KUO ET AL.

Examiner

Amy He

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 February 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-5 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter (U. S. Pub. 2004/;0004488) in view of applicant's admitted prior art (hereafter AAP)(Figures 1-4; or see the section of related art in the instant specification).

As for claims 1 and 2, Baxter discloses a method/circuit (in Figure 13) for measuring capacitance, comprising:

providing a first switch (65), wherein a terminal of the first switch (65) is connected to a terminal of a first capacitor (64);

providing a second switch (62), wherein a terminal of the second switch(62) is connected to a terminal of a second capacitor (63);

providing a third switch (66), wherein a terminal of the third switch (66) is connected to another terminal of the first capacitor (64) and another terminal of the second capacitor (63).

Baxter does not disclose providing a P-type transistor, wherein a gate of the P-type transistor is connected to another terminal of the third switch; and wherein when the first switch, the second switch and the third switch are turned on, a capacitance of

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the first capacitor, a capacitance of the second capacitor, or a ratio of a difference between the capacitance of first capacitor and the capacitance of the second capacitor to an average of the capacitance of first capacitor and the capacitance of the second capacitor is measured via the another terminal of the first switch, the another terminal of the second switch, and a source and a drain of the P-type transistor.

AAP discloses providing a P-type transistor (PMOS in Figures 1, 3 and 4), wherein a gate of the P-type transistor is connected to a second terminal of a first capacitor (102) and a second capacitor (104); and measuring a capacitance of the first capacitor, a capacitance of the second capacitor, or a ratio of a difference between the capacitance of first capacitor and the capacitance of the second capacitor to an average of the capacitance of first capacitor and the capacitance of the second capacitor via the another terminal of the first switch, the another terminal of the second switch, and a source and a drain of the P-type transistor (see pages 2-3 of the instant specification).

A person of ordinary skill in the art would find it obvious at the time the invention was made to modify Baxter to incorporate the use of a P-type transistor and the method for measuring the capacitances in a capacitor pair, as taught by AAP, so that a gate of the P-type transistor is connected to the another terminal of the third switch (66), and wherein when the first switch, the second switch and the third switch are turned on, a capacitance of the first capacitor, a capacitance of the second capacitor, or a ratio of a difference between the capacitance of first capacitor and the capacitance of the second capacitor to an average of the capacitance of first capacitor and the capacitance of the second capacitor is measured via the another terminal of the first switch, the another

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terminal of the second switch, and a source and a drain of the P-type transistor, as taught by AAP, for the purpose of measuring the capacitances and the capacitance mismatch of the capacitor pair of Baxter (i.e. the capacitor pair composed of 63 and 64) with good rejection of ambient noise.

As for claims 3-5 and 9-11, Baxter discloses the method/circuit as in claims 1 and 2. Baxter does not disclose a plurality of capacitor pairs and providing a plurality of first switches, a plurality of second switches and a plurality of third switches; and providing a P-type transistor, wherein a gate of the P-type transistor is connected to another terminal of the third switches of all the capacitor pairs, wherein when the first switch, the second switch and the third switch are turned on, a capacitance of the first capacitor, a capacitance of the second capacitor, or a ratio of a difference between the capacitance of first capacitor and the capacitance of the second capacitor to an average of the capacitance of first capacitor and the capacitance of the second capacitor is measured via a first pad, a second pad and a source and drain of the P-type transistor.

AAP discloses providing a P-type transistor (PMOS in Figures 1, 3 and 4), wherein a gate of the P-type transistor is connected to a second terminal of a first capacitor (102) and a second capacitor (104); and measuring a capacitance of the first capacitor, a capacitance of the second capacitor, or a ratio of a difference between the capacitance of first capacitor and the capacitance of the second capacitor to an average of the capacitance of first capacitor and the capacitance of the second capacitor via a first pad, a second pad and a source and drain of the P-type transistor (see pages 2-3 of the instant specification).

A person of ordinary skill in the art would find it obvious at the time the invention was made to modify Baxter to incorporate the use of a P-type transistor and the method for measuring the capacitances in a capacitor pair, as taught by AAP, so that a gate of the P-type transistor is connected to the another terminal of the third switch (66), and wherein when the first switch, the second switch and the third switch are turned on, a capacitance of the first capacitor, a capacitance of the second capacitor, or a ratio of a difference between the capacitance of first capacitor and the capacitance of the second capacitor to an average of the capacitance of first capacitor and the capacitance of the second capacitor is measured via a first pad, a second pad and a source and drain of the P-type transistor, as taught by AAP, for the purpose of measuring the capacitances and the capacitance mismatch of the capacitor pair of Baxter (i.e. the capacitor pair composed of capacitor 63 and 64) with good rejection of ambient noise.

In addition, the person of ordinary skill in the art would also find it obvious at the time of the invention to modify Baxter to disclose using a plurality of the first switches, a plurality of the second switches and a plurality of the third switches in a plurality of capacitor pairs, so that the gate of the P-type transistor is connected to another terminal of all the third switches of all the capacitor pairs, for the purpose of measuring the capacitances and the capacitance mismatch of the plurality of capacitor pairs with good rejection of ambient noise, and since it has been held that mere duplication of the essential working parts (first switch, second switch and third switch of a capacitor pair) of a device involves only routine skill in the art. *See In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

2. Claims 6-8 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter (U. S. Pub. 2004/0004488) in view of applicant's admitted prior art (hereafter AAP)(Figures 1-4; or see the section of related art in the instant specification), and further in view of Morishige et al. (U. S. Pub. No. 2006/0214890).

As for claims 6, 8, 12 and 14, Baxter in view of AAP discloses the method/circuit as applied to claims 3 and 9 above. Baxter in view of AAP lacks a selection circuit/a shift register, connected to all of the first switches, the second switches and the third switches to selectively turn on or turn off the first switches, the second switches or the third switches.

Morishige et al. discloses a selection circuit/a shift register (5 in Figure 1 or 103 in Figure 9), connected to a plurality of second switches, for the purpose of sequentially selecting a plurality of second switches (see claim 20).

A person of ordinary skill in the art would find it obvious at the time of the invention to further modify Baxter in view of AAP to use a conventional selection circuit/shift register, as taught by Morishige et al., to connect to all of the first switches, the second switches and the third switches, for the purpose of selectively turn on or turn off the first switches, the second switches or the third switches sequentially (see claim 20).

As for claims 7 and 13, Baxter in view of AAP and further in view of Morishige et al. discloses the method/circuit as applied to claims 6 and 12 above. Baxter in view of

AAP and further in view of Morishige et al. lacks a step of automatically operating the method.

However, broadly providing an automating step to replace a manual activity that accomplished the same result is not sufficient to distinguish over the prior art. See *in re Venner*, 262 F.2d 91, 95, 120 USPQ 193, 194 (CCPA 1958).

A person of ordinary skill in the art at the time of the invention would find it obvious to further modify Baxter in view of AAP and Morishige et al. to include this automating step to sequentially measure the capacitances in the plurality of capacitor pairs.

Response to Arguments

3. Applicant's arguments filed February 6, 2007 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., when the third switch 524c is not turned on yet, the gate of the P-type transistor is floating, and another terminal of the third switch 524c is disconnected to another terminal of the first capacitor 522a and the second capacitor 522b) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amy He whose telephone number is (571) 272-2230. The examiner can normally be reached on 8:30am-5pm.

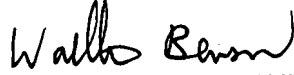
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Hirshfeld can be reached on 571-272-2168. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

April 18, 2007.


WALTER BENSON, PHD, P.E.
PRIMARY EXAMINER